TECHNIQUE TO CONTROL TUNNELING CURRENTS IN DRAM CAPACITORS, CELLS, AND DEVICES

Abstract of the Disclosure

5 Structures and methods are provided for the use with PMOS devices.

Materials with large electron affinities or work functions are provided for structures such as gates. A memory cell is provided that utilizes materials with work functions larger than n-type doped polysilicon (4.1 eV) or aluminum metal (4.1 eV) for gates or capacitor plates.